

What is claimed is:

- 1    1.     A circuit comprising:  
2                at least one phase lock loop to generate at least one core signal having  
3 multiple cycles within one cycle of an external signal;  
4                a ratio decoder to decode a programming code; and  
5                an alignment unit coupled to the at least one phase lock loop and the  
6 ratio decoder to synchronize a plurality of propagation pulses with the external  
7 signal based on the programming code.
- 1    2.     The circuit of claim 1, wherein the alignment unit includes a master pulse  
2 generator to generate a master pulse having a pulse width equal to one cycle of the  
3 at least one core signal.
- 1    3.     The circuit of claim 1, wherein the alignment unit includes a propagation  
2 pulse generator to periodically provide each of the propagation pulses to an  
3 propagation compensator of the alignment unit at a propagation interval before an  
4 occurrence of an anticipated edge of the external clock.
- 1    4.     The circuit of claim 3, wherein the propagation pulse generator includes a  
2 counter and a reset unit coupled to the counter to reset the counter after a first  
3 propagation pulse among the plurality of propagation pulses is generated.
- 1    5.     The circuit of claim 1, wherein the ratio decoder includes a math unit to  
2 perform a math operation on the programming code.
- 1    6.     The circuit of claim 5, wherein the ratio decoder further includes a selector  
2 to select between a control value represented by a programming code and a control  
3 value resulted from the math operation.

1     7.     An integrated circuit comprising:  
2             a phase lock loop network to receive an external signal to generate at least  
3     one core signal;  
4             a master pulse generator to generate a master pulse based on a combination  
5     of the at least core signal and a modified version of the external signal;  
6             a propagation pulse generator coupled to the master pulse generator to  
7     generate a plurality of propagation pulses based on the master pulse;  
8             an propagation compensator coupled to the propagation pulse generator to  
9     propagate the plurality of propagation pulses for a propagation interval to generate  
10    an internal clock signal; and  
11            a ratio decoder coupled to the propagation pulse generator to provide at least  
12    one control value to influence a timing of the plurality of propagation pulses.

1     8.     The integrated circuit of claim 7, wherein the master pulse generator  
2     includes a logic unit to enable a pulse width of the master pulse to be one cycle of  
3     the at least one core signal.

1     9.     The integrated circuit of claim 8, wherein the master pulse generator further  
2     includes a reset unit to reset the master pulse generator.

1     10.    The integrated circuit of claim 7, wherein the propagation pulse generator  
2     includes a counter coupled to the master pulse generator.

1     11.    The integrated circuit of claim 10, wherein the counter is a ring counter.

1     12.    The circuit of claim 7, wherein the ratio decoder includes a logic circuit to  
2     perform a subtraction operation on the at least one control value.

1     13.    The circuit of claim 12, wherein the ratio decoder further includes a selector  
2     to select the at least one control value.

1 14. The integrated circuit of claim 7, wherein the propagation compensator  
2 includes a plurality of flip-flops coupled in series between an output node of the  
3 propagation pulse generator and an output node of the propagation compensator.

1 15. The integrated circuit of claim 7 further comprising at least one component  
2 coupled to the propagation compensator to receive the internal signal.

1 16. A system comprising:  
2 a clock generator to generate an external signal;  
3 a dynamic random access memory device coupled to receive the clock  
4 generator; and  
5 a plurality of integrated circuits coupled to receive the external signal, at  
6 least one of the plurality of integrated circuits including:  
7 an internal signal generating unit to generate at least one core signal;  
8 a ratio decoder to decode a programming code; and  
9 an alignment unit coupled to the internal signal generating unit and the  
10 ratio decoder to synchronize a plurality of propagation pulses with the external  
11 signal based on the programming code.

1 17. The system of claim 16, wherein the internal signal generating unit  
2 include multiple phase lock loops coupled in a cascaded configuration.

1 18. The system of claim 16, wherein one of the integrated circuit includes a  
2 processor.

1 19. The system of claim 16, wherein the alignment unit includes a master pulse  
2 generator to generate a master pulse having a pulse width equal to at least one cycle  
3 of the at least one core signal.

1 20. The system of claim 16, wherein the alignment unit includes a propagation  
2 pulse generator to periodically provide each of the propagation pulses to an  
3 propagation compensator of the alignment unit at a propagation interval before an  
4 occurrence of an anticipated edge of the external clock.

1 21. The system of claim 16, wherein the ratio decoder includes a logic unit to  
2 perform a math operation on the programming code.

1 22. The system of claim 21, wherein the ratio decoder further includes a selector  
2 to select between a control value represented by a programming code and a control  
3 value resulted from the math operation.

1 23. A method comprising:  
2 generating a core signal based on an external signal, the core signal having  
3 core cycles;  
4 producing a master pulse based on a combination of the core signal and a  
5 modified version of the external signal;  
6 producing a plurality of propagation pulses including a first propagation  
7 pulse and a group of subsequent propagation pulses, wherein the first propagation  
8 pulse is produced at an initial interval after the master pulse is produced; and  
9 propagating the plurality of propagation pulses for a propagation interval to  
10 align the plurality of propagation pulses with the external signal.

1 24. The method of claim 23 further comprising setting a reference value,  
2 wherein the reference value represents a number of the core cycles within one cycle  
3 of the external signal.

1 25. The method of claim 23, wherein the master pulse having a pulse width,  
2 wherein the pulse width equals an interval between two consecutive rising edges of  
3 the core signal.

1    26.    The method of claim 23, wherein the initial interval is a variable value.

1    27.    The method of claim 23, wherein the propagation interval is an interval  
2    between an occurrence of one of the propagation pulses and an occurrence of an  
3    anticipated edge of the external clock signal.

1    28.    The method of claim 23, wherein the initial interval includes a number of  
2    initial core cycles, wherein a number of initial core cycles is less than a number of  
3    core cycles within one cycle of the external clock signal.

1    29.    The method of claim 28, wherein each of the subsequent propagation pulses  
2    is produced at a multiple of the number of core cycles within one cycle of the  
3    external clock after the first propagation pulse is produced.